AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (previously presented) A method of operation within an integrated circuit device, the method comprising:

generating an index based on a search value;

determining whether constituent bits of the search value, including bits thereof used to generate the index, match corresponding bits of a data value stored at a memory location indicated by the index; and

outputting, from the integrated circuit device, the index and an indication of whether the constituent bits of the search value match the corresponding bits of the data value.

2. (original) The method of claim 1 wherein generating the index based on the search value comprises selecting a portion of the search value, and generating the index based on the selected portion of the search value.

3. (original) The method of claim 2 wherein selecting the portion of the search value comprises selecting the portion of the search value in accordance with a configuration value stored within the integrated circuit device.

4. (original) The method of claim 1 wherein generating an index based on the search value comprises:

assembling dispersed fields of bits within the search value to form a search key; and

generating the index based on the search key.

5. (original) The method of claim 4 further comprising masking selected bits within the search key prior to generating the index.

6. (original) The method of claim 5 wherein masking selected bits within the search key comprises masking bits within the search key in accordance with a configuration value within the integrated circuit device.

7. (original) The method of claim 4 wherein assembling dispersed fields of bits within the search value to form the search key comprises assembling the dispersed fields of bits into a contiguous set of bits in accordance with a configuration value within the integrated circuit device.

8. (original) The method of claim 7 wherein the configuration value specifies a data format of the search value.

9. (original) The method of claim 1 wherein generating the index based on the search value comprises generating a hash index based on the search value, the hash index having fewer constituent bits than the search value.

10. (original) The method of claim 9 wherein generating the hash index comprises generating a cyclic redundancy check (CRC) value.

11. (original) The method of claim 1 wherein determining whether the search value matches the data value comprises comparing the search value with the data value to generate a match signal that indicates whether the search value matches the data

value.

12. (original) The method of claim 11 wherein outputting the indication of whether the search value matches the data value comprises outputting the match signal.

13. (original) The method of claim 11 wherein comparing the search value with the data value comprises comparing a selected portion of the search value with a selected portion of the data value, the selected portions of the search value and data value being indicated by a mask value.

14. (original) The method of claim 13 further comprising retrieving the mask value from the memory location indicated by the index.

15. (original) The method of claim 13 further comprising decoding an encoded value to generate the mask value.

16. (original) The method of claim 15 further comprising retrieving the encoded value from the memory location indicated by the index.

17. (original) The method of claim 11 wherein comparing the search value with the data value comprises determining whether the search value is greater than the data value and wherein generating the match signal that indicates whether the search value matches the data value comprises generating a match signal to indicate that the search value matches the data value if the search value is not greater than the data value.

18. (original) The method of claim 11 wherein comparing the search value with the data value comprises determining whether the search value is less than the data value and wherein generating the match signal that indicates whether the search value matches the data value comprises generating a match signal to indicate that the search value matches the data value if the search value is not less than the data value.

19. (original) The method of claim 11 wherein comparing the search value with the data value comprises performing either a range comparison or a match comparison according to a configuration value within the integrated circuit device, and wherein performing a range comparison comprises determining whether the search value is greater than the data value.

20. (original) The method of claim 1 wherein generating an index based on a search value comprises:

generating a plurality of hash values based on the search value, each hash value having fewer constituent bits than the search value; and

selecting one of the hash values to be the index.

21. (original) The method of claim 20 wherein selecting one of the hash values to be the index comprises selecting the one of the hash values in accordance with a configuration value within the integrated circuit device.

22. (original) The method of claim 1 further comprising:

retrieving a priority value from the memory location indicated by the index; and

outputting the priority value from the integrated circuit device.

23. (canceled)

24. (currently amended) A method of operation within an integrated circuit device, the method comprising:

receiving a search value;

generating an index based on a selected bits of the search value;

determining whether constituent bits of the search value, including the selected bits, match corresponding bits of a data value stored at a memory location indicated by the index; and

~~The method of claim 23 further comprising~~ selecting the selected bits of the search value in accordance with a configuration value stored within the integrated circuit device.

25. (currently amended) A method of operation within an integrated circuit device, the method comprising:

receiving a search value;

generating an index based on a selected bits of the search value;

determining whether constituent bits of the search value, including the selected bits, match corresponding bits of a data value stored at a memory location indicated by the index; and

~~The method of claim 23~~ wherein generating an index based on selected bits of the search value comprises:

assembling dispersed fields of bits within the search value to form a search

key; and

generating the index based on the search key.

26. (previously presented) The method of claim 25 further comprising masking bits within the search key prior to generating the index.

27. (previously presented) The method of claim 26 wherein masking bits within the search key comprises masking bits within the search key in accordance with a configuration value within the integrated circuit device.

28. (original) The method of claim 25 wherein assembling dispersed fields of bits within the search value to form the search key comprises assembling the dispersed fields of bits into a contiguous set of bits in accordance with a configuration value within the integrated circuit device.

29. (currently amended) The method of claim ~~23~~ 24 wherein generating the index based on selected bits of the search value comprises generating a hash index based on the selected bits of the search value, the hash index having fewer constituent bits than the search value.

30. (original) The method of claim 29 wherein generating the hash index comprises generating a cyclic redundancy check (CRC) value.

31. (canceled)

32. (canceled)

33. (currently amended) A method of operation within an integrated circuit device, the method comprising:

generating an index based on a search value;

generating an indication of whether a first portion of the search value, including constituent bits of the search value used to generate the index, matches a selected portion of a data value stored at a memory location indicated by the index; and

wherein generating the index based on the search value comprises selecting a portion of the first portion of the search value, and generating the index based on the selected portion of the first portion of the search value, and ~~The method of claim 32~~ wherein selecting the portion of the first portion of the search value comprises selecting the portion of the first portion of the search value in accordance with a configuration value stored within the integrated circuit device.

34. (currently amended) A method of operation within an integrated circuit device, the method comprising:

generating an index based on a search value;

generating an indication of whether a first portion of the search value, including constituent bits of the search value used to generate the index, matches a selected portion of a data value stored at a memory location indicated by the index; and

~~The method of claim 31~~ wherein generating an index based on the search value comprises:

assembling dispersed fields of bits within the search value to form a search key; and

generating the index based on the search key.

35. (previously presented) The method of claim 34 further comprising masking selected bits within the search key prior to generating the index, the selected bits being selected in accordance with a configuration value within the integrated circuit device.

36. (currently amended) The method of claim ~~31~~ 33 wherein generating an indication of whether a first portion of the search value matches a selected portion of a data value stored at a memory location indicated by the index comprises:

retrieving the data value from the memory location indicated by the index; and

comparing the first portion of the search value with the selected portion of the data value to generate a match signal that indicates whether the search value matches the data value.

37. (currently amended) A method of operation within an integrated circuit device, the method comprising:

generating an index based on a search value;

generating an indication of whether a first portion of the search value, including constituent bits of the search value used to generate the index, matches a selected portion of a data value stored at a memory location indicated by the index;

~~The method of claim 36 further comprising~~ retrieving mask information from the

memory location indicated by the index, the mask information indicating the selected portion of the data value; and

wherein generating the indication of whether the first portion of the search value matches the selected portion of the data value stored at the memory location indicated by the index comprises:

retrieving the data value from the memory location indicated by the index; and

comparing the first portion of the search value with the selected portion of the data value to generate the match signal that indicates whether the search value matches the data value.

38. (original) The method of claim 37 further comprising decoding an encoded value included within the mask information to generate a decoded mask value, the mask value indicating the selected portion of the data value.

39. (original) A method of operation within an integrated circuit device the method comprising:

generating a search index based on a search value; and

identifying, within a content addressable memory (CAM), one of a plurality of stored indices that matches the search index; and

determining whether the search value matches a data value stored at a first location within a data memory, the first location corresponding to a location of the one of the plurality of indices.

40. (original) The method of claim 39 wherein generating the search index based on

the search value comprises selecting a portion of the search value, and generating the search index based on the selected portion of the search value.

41. (original) The method of claim 40 wherein selecting the portion of the search value comprises selecting the portion of the search value in accordance with a configuration value within the integrated circuit device.

42. (original) The method of claim 39 wherein generating the search index based on the search value comprises generating a search index having fewer constituent bits than the search value.

43. (original) The method of claim 39 wherein generating the search index comprises generating a cyclic redundancy check (CRC) value.

44. (original) The method of claim 39 wherein identifying, within the CAM, one of a plurality of stored indices that matches the search index comprises comparing the search index with each of the plurality of stored indices.

45. (original) The method of claim 44 wherein comparing the search index with each of the plurality of stored indices comprises simultaneously comparing the search index with each of the plurality of stored indices.

46. (original) The method of claim 44 wherein identifying one of a plurality of stored indices that matches the search index further comprises generating a plurality of match signals, each match signal indicating whether a respective one of the stored indices matches the search index.

47. (original) The method of claim 39 wherein determining whether the search value matches a data value stored at a first location within a data memory comprises:
retrieving the data value from the first location within the memory; and
comparing the search value with the data value.

48. (original) The method of claim 47 wherein retrieving the data value from the first location within the memory comprises:
generating a row address indication that corresponds to the one of the plurality of stored indices that matches the search index; and
retrieving the data value from a location within the memory indicated by the row address indication.

49. (original) The method of claim 48 wherein generating the row address indication comprises generating a plurality of match signals that each indicate whether a respective one of the stored indices matches the search index.

50. (original) The method of claim 49 wherein generating the row address indication further comprises encoding the plurality of match signals into a row address.

51. (original) The method of claim 50 wherein encoding the plurality of match signals into a row address comprises retrieving the row address from a lookup table storage location indicated by the plurality of match signals.

52. (original) A method of operation within an integrated circuit device, the method comprising:

converting a search value into a search index having fewer constituent bits than the search value;

identifying, within a content addressable memory (CAM), one of a plurality of stored indices that matches the search index; and

outputting a data value from a first location within a data memory, the first location corresponding to a location within the CAM of the one of the plurality of indices.

53. (original) The method of claim 52 further comprising determining whether the search value matches the data value.

54. (original) The method of claim 53 further comprising generating a match signal that indicates whether the search value matches the data value.

55. (original) The method of claim 52 wherein converting a search value into a search index comprises converting a selected portion of the search value into a search index.

56. (original) The method of claim 52 wherein converting a search value into a search index comprises generating a hash index based on the search value.

57. (original) The method of claim 56 wherein generating a hash index comprises generating a cyclic redundancy check (CRC) value.

58. (original) The method of claim 52 wherein identifying, within the CAM, one of a plurality of stored indices that matches the search index comprises comparing the

search index with each of the plurality of stored indices.

59. (original) The method of claim 58 wherein comparing the search index with each of the plurality of stored indices comprises simultaneously comparing the search index with each of the plurality of stored indices.

60. (original) The method of claim 58 wherein identifying, within a content addressable memory (CAM), one of a plurality of stored indices that matches the search index further comprises generating a plurality of match signals, each match signal indicating whether a respective one of the stored indices matches the search index.

61. (original) The method of claim 52 wherein outputting the data value from the first location within the data memory comprises:

generating a row address indication that corresponds to the one of the plurality of stored indices that matches the search index; and

retrieving the data value from a location within the data memory indicated by the row address indication.

62. (original) The method of claim 61 wherein generating the row address indication comprises generating a plurality of match signals that each indicate whether a respective one of the stored indices matches the search index.

63. (original) The method of claim 62 wherein generating the row address indication further comprises encoding the plurality of match signals into a row address.

64. (original) A method of operation within an integrated circuit device, the method comprising:

generating a plurality of indices based on a search value;

selecting, according to a select value, one of the plurality of indices; and

determining whether the search value matches a data value stored at a memory location indicated by the one of the plurality of indices.

65. (original) The method of claim 64 wherein generating a plurality of indices based on a search value comprises selecting a portion of the search value, and generating each of the plurality of indices based on the selected portion of the search value.

66. (original) The method of claim 65 wherein selecting the portion of the search value comprises selecting the portion of the search value in accordance with a configuration value stored within the integrated circuit device.

67. (original) The method of claim 65 wherein generating each of the plurality of indices based on the search value comprises:

assembling dispersed fields of bits within the search value to form a search key; and

generating each of the plurality of indices based on the search key.

68. (original) The method of claim 67 further comprising masking selected bits within the search key prior to generating the plurality of indices.

69. (original) The method of claim 68 wherein masking selected bits within the search key comprises masking bits within the search key in accordance with a

configuration value within the integrated circuit device.

70. (original) The method of claim 64 wherein selecting one of the plurality of indices comprises selecting one of the plurality of indices in accordance with a configuration value within the integrated circuit device.

71. (original) The method of claim 64 wherein generating a plurality of indices based on a search value comprises generating a plurality of different indices based on the search value.

72. (original) The method of claim 71 wherein generating a plurality of plurality of different indices comprises inputting at least a portion of the search value to a plurality of hash function circuits, each hash function circuit being adapted to generate a respective hash index based on a hash function that is different from the others of the hash function circuits.

73. (original) The method of claim 64 wherein determining whether the search value matches a data value stored at a memory location indicated by the one of the plurality of indices comprises comparing the search value with the data value and generating a match signal that indicates whether the search value matches the data value.

74. (original) The method of claim 73 wherein comparing the search value with the data value comprises comparing a selected portion of the search value with a selected portion of the data value, the selected portions of the search value and data value being indicated by a mask value.

75. (original) The method of claim 74 further comprising retrieving the mask value from the memory location indicated by the one of the plurality of indices.

76. (original) A method of operation within an integrated circuit device, the method comprising:

generating a plurality of indices based on a search value;

retrieving a plurality of data values from a plurality of memories, each data value being retrieved from a respective one of the memories at a location indicated by a respective one of the plurality of indices;

comparing the search value to each of the plurality of data values to identify one of the data values that matches the search value; and

generating a value that identifies the respective one of the memories from which the one of the data values that matches the search value was retrieved.

77. (original) The method of claim 76 wherein generating a plurality of indices based on a search value comprises generating a plurality of hash indices based on at least a portion of the search value, each of the hash indices having fewer constituent bits than the search value.

78. (original) The method of claim 77 wherein generating the plurality of hash indices comprises generating a plurality of cyclic redundancy check (CRC) values.

79. (original) The method of claim 76 wherein comparing the search value to each of the plurality of data values comprises comparing the search value with a selected portion of each of the data values, the selected portion of each of the data values

being indicated by a respective mask value.

80. (original) The method of claim 79 further comprising retrieving the respective mask value from a respective one of the memories at a location indicated by a respective one of the plurality of indices.

81. (original) The method of claim 76 wherein retrieving a plurality of data values from a plurality of memories comprises retrieving a first data value from a first one of the plurality of memories, and retrieving a second data value from a second one of the plurality of memories, the second one of the plurality of memories having a different storage capacity than the first one of the plurality of memories.

82. (original) A method of operation within an integrated circuit device, the method comprising:

receiving a search value and a corresponding search code;

comparing the search code to a plurality of configuration values, each of the configuration values corresponding to a respective one of a plurality of data memories within the integrated circuit device;

generating a plurality of indices based on the search value;

retrieving a plurality of data values from the plurality of data memories, each data value being retrieved from a respective one of the data memories at a location indicated by a respective one of the indices; and

generating, for each of the plurality of data memories, a respective match signal having a first state if the search value matches the data value retrieved from the data memory and if the search code matches the configuration value that

corresponds to the data memory.

83. (original) The method of claim 82 wherein receiving a search code comprises receiving a search code that indicates a formatting of the corresponding search value.

84. (original) The method of claim 82 wherein receiving a search code comprises receiving a search code that indicates positions of maskable bits within the corresponding search value.

85. (original) The method of claim 82 wherein generating a match signal having a first state if the search value matches the data value retrieved from the data memory and if the search code matches the configuration value that corresponds to the data memory comprises:

comparing a selected portion of the search value and a selected portion of the data value; and

generating a match signal having a first state if the selected portion of the search signal matches the selected portion of the data value and if the search code matches the configuration value.

86. (original) The method of claim 82 further comprising retrieving a plurality of priority values from the plurality of data memories, each priority value being retrieved from a respective one of the data memories at a location indicated by a respective one of the indices.

87. (original) The method of claim 82 further comprising generating an identifier based

on the plurality of priority values and the match signals generated for the plurality of data memories, the identifier indicating one of the plurality of data memories.

88. (original) The method of claim 87 wherein generating an identifier that indicates one of the plurality of data memories comprises generating an identifier that indicates a data memory of the plurality of data memories that contains a highest priority one of the plurality of priority values and for which the respective match signal has the first state.

89. (original) A method of operation within an integrated circuit device, the method comprising:

generating an index based on an input value;

retrieving a first value from a location, indicated by the index, within a first memory;

comparing the first value to the input value to generate a first match signal that indicates whether the input value matches the first value; and

comparing the input value simultaneously to each of a plurality of values stored in a second memory to generate a second match signal that indicates whether the input value matches one of the plurality of values stored in the second memory.

90. (original) The method of claim 89 wherein comparing the input value simultaneously to each of a plurality of values stored in the second memory comprises comparing the input value to a plurality of values stored in an array of content addressable memory (CAM) cells, each CAM cell including a storage

element and a compare circuit.

91. (original) The method of claim 89 further comprising:
outputting a first priority value from the location within the first memory;
outputting a second priority value from the second memory; and
comparing the first priority value and the second priority value in accordance with the states of the first and second match signals to determine a highest priority one of the priority values.

92. (original) The method of claim 91 wherein comparing the first priority value and the second priority value in accordance with the states of the first and second match signals to determine a highest priority one of the priority values comprises determining the first priority value to be the highest priority value if the first match signal is asserted and the first priority value indicates a higher priority than the second priority value.

93. (original) The method of claim 89 wherein generating an index based on an input value comprises generating an index having fewer constituent bits than the input value.

94. (original) The method of claim 89 wherein generating the index based on the search value comprises selecting a portion of the search value, and generating the index based on the selected portion of the search value.

95. (original) The method of claim 94 wherein selecting the portion of the search value comprises selecting the portion of the search value in accordance with a

configuration value within the integrated circuit device.

96. (original) The method of claim 94 wherein generating an index based on the search value comprises:

assembling dispersed fields of bits within the search value to form a search key; and

generating the index based on the search key.

97. (original) The method of claim 96 further comprising masking selected bits within the search key prior to generating the index.

98. (original) The method of claim 97 wherein masking selected bits within the search key comprises masking bits within the search key in accordance with a configuration value within the integrated circuit device.

99. (original) A method of operation within an integrated circuit device, the method comprising:

generating a plurality of priority values in response to a first instruction, each priority value indicating a storage capacity of a respective one of a plurality of circuit blocks; and

generating, based on the priority values, a block identifier that identifies one of the circuit blocks.

100. (previously presented) The method of claim 99 wherein generating the block identifier based on the priority values comprises generating a block identifier that identifies a least filled one of the plurality of circuit blocks.

101. (original) The method of claim 99 wherein generating the block identifier based on the priority values comprises generating a block identifier that identifies a most filled one of the plurality of circuit blocks.

102. (original) The method of claim 99 further comprising storing, in response to generation of the block identifier, a data value in the one of the plurality of circuit blocks identified by the block identifier.

103. (original) A method of operation within an integrated circuit device, the method comprising:

generating a plurality of indices based on a search value; and

for each of a plurality of circuit blocks within the integrated circuit device:

selecting one of the indices;

retrieving a data value from a first storage location within the circuit block, the first storage location being indicated by the one of the indices; and

determining whether the data value matches the search value.

104. (original) The method of claim 103 wherein generating the plurality of indices based on the search value comprises generating a plurality of indices that each have fewer constituent bits than the search value.

105. (original) The method of claim 103 wherein generating the plurality of indices based on the search value comprises generating each of the plurality of indices based on a selected portion of the search value.

106. (original) The method of claim 103 wherein selecting one of the indices comprises selecting one of the indices in accordance with a configuration value within the integrated circuit.

107. (original) The method of claim 103 wherein determining whether the data value matches the search value comprises comparing a selected portion of the data value with a selected portion of the mask value.